# (19) World Intellectual Property Organization

International Bureau



# | COLIN DIVIDUS | 1 COLING VIAN DOWN BOOK BIN | 1 N W BOILD WHI 1856 | 1910 BIN BIN 1876 | 1956 | 1957 | 1957

### (43) International Publication Date 7 April 2005 (07.04.2005)

**PCT** 

## (10) International Publication Number WO 2005/031859 A1

(51) International Patent Classification7: H01L 21/8247. 21/28, 27/115, 21/336, 29/788

(21) International Application Number:

PCT/IB2004/051795

(22) International Filing Date:

20 September 2004 (20.09.2004)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data: 03103607.2

30 September 2003 (30.09.2003)

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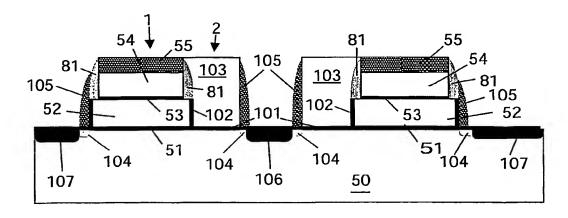
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: 2-TRANSISTOR MEMORY CELL AND METHOD FOR MANUFACTURING



(57) Abstract: The present invention provides a method of manufacturing on a substrate (50) a 2-transistor memory cell comprising a storage transistor (1) having a memory gate stack (1) and a selecting transistor, there being a tunnel dielectric layer (51) between the substrate (50) and the memory gate stack. (1). The method comprises forming the memory gate stack (1) by providing a first conductive layer (52) and a second conductive layer (54) and etching the second conductive layer (54) thus forming a control gate and etching the first conductive layer (52) thus forming a floating gate. The method is characterized in that it comprises, before etching the first conductive layer (52), forming spacers (81) against the control gate in the direction of a channel to be formed under the tunnel dielectric layer (51), and thereafter using the spacers (81) as a hard mask to etch the first conductive layer (52) thus forming the floating gate, thus making the floating gate self aligned with the control gate. The present invention also provides a memory cell wherein the control gate (54) is smaller than the floating gate (52), and spacers (81) are present next to the control gate (54).

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#### Declaration under Rule 4.17:

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IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

#### Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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